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METHOD FOR FABRICATING A HARD MASK POLYSILICON GATE

Field of the Invention

[001] The present invention relates generally to fabrication of polysilicon gates in a semiconductor device. More particularly, the present invention relates to a method for fabricating a hard mask polysilicon gate using a fluorine-based etch followed by a non-fluorine based etch, to eliminate a necking profile from the polysilicon gate.

Background of the Invention

[002] The fabrication of various solid state devices requires the use of planar substrates, or semiconductor wafers, on which integrated circuits are fabricated. The final number, or yield, of functional integrated circuits on a wafer at the end of the IC fabrication process is of utmost importance to semiconductor manufacturers, and increasing the yield of circuits on the wafer is the main goal of semiconductor fabrication. After packaging, the circuits on the wafers are tested, wherein non-functional dies are marked using an inking process and the functional dies on the wafer are separated and sold. IC fabricators increase the yield of dies on a wafer by exploiting economies of scale. Over 1000 dies may be formed on a single wafer which measures from six to twelve inches in diameter.

[003] Various processing steps are used to fabricate integrated circuits on a semiconductor wafer. These steps include sequential deposition of conductive and insulative layers on the silicon wafer substrate; formation of a photoresist or other mask such as titanium oxide or silicon oxide, in the form of the desired metal interconnection pattern, using standard lithographic or photolithographic techniques; subjecting the wafer substrate to a dry etching process to remove material from one or more conducting layers from the areas not covered by the mask, thereby etching the conducting layer or layers in the form of the masked pattern on the substrate; removing or stripping the mask layer from the substrate typically using reactive plasma and chlorine gas, thereby exposing the top surface of the conductive interconnect layer; and cooling and drying the wafer substrate by applying water and nitrogen gas to the wafer substrate.

[004] The numerous processing steps outlined above are used to cumulatively apply multiple electrically conductive and insulative layers on the wafer and pattern the layers to form the circuits. Additional techniques, such as dual damascene processes, are used to form conductive vias which establish electrical contact between vertically-spaced conductive lines or layers in the circuits. The finished semiconductor product includes microelectronic devices including transistors,

capacitors and resistors that form the integrated circuits on each of multiple die on a single wafer.

[005] In the semiconductor industry, CMOS (complementary metal-oxide semiconductor) technology is extensively used in the fabrication of IC devices. CMOS technology typically involves the use of overlying layers of semiconductor material with the bottom layer being a dielectric layer and the top layer being a layer of doped silicon material that serves as a low- resistivity electrical contact gate electrode. The gate electrode, also referred to as a gate stack, typically overlies the dielectric layer.

[006] In the semiconductor fabrication industry, silicon oxide (SiO_2) is frequently used for its insulating properties as a gate oxide or dielectric. As the dimensions of device circuits on substrates become increasingly smaller, the gate dielectric thickness must decrease proportionately in field effect transistors (FETs) to approximately 3 to 3.5 nonometers. Accordingly, device performance and reliability can be adversely affected by such factors as interfacial defects, defect precursors and diffusion of dopants through gate dielectrics, as well as unintended variations in thickness in the gate oxide layer among central and peripheral regions of the layer.

[007] As microelectronic fabrication integration levels have increased and patterned microelectronic conductor layer dimensions have decreased, it has become increasingly important within the art of microelectronic fabrication to form within microelectronic fabrications patterned microelectronic conductor layers, such as but not limited to gate electrodes within field effect transistors (FETs), as well as patterned microelectronic conductor interconnect layers, with a uniform sidewall profile. Uniform sidewall profiles are particularly desirable within gate electrodes in field effect transistors since gate electrode linewidth and profile define operational parameters of the integrated circuit within which is formed the FET. While a uniform sidewall profile is thus desirable in gate electrodes and other structures in IC devices, uniform sidewalls are, in many cases, not readily achievable.

[008] A typical conventional process for patterning a polysilicon gate using a hard mask is shown in Figures 1A and 1B. A multi-layered semiconductor structure 10, shown in Figure 1A, is initially fabricated on a substrate 12 by sequentially depositing a gate oxide layer 14, a polysilicon layer 16, a hard mask layer 18, a bottom anti-reflective coating (BARC) layer 20, and a resist layer 22 on the substrate 12. Next, the BARC layer 20 and the hard mask layer 18 are etched according to the

patterned PR layer 22. This is followed by stripping of the PR layer 22 and the underlying BARC layer 20 from the patterned hard mask layer 18, to form the portion of the structure 10 which is defined by the solid lines in Figure 1A.

[009] Next, the polysilicon layer 16 is etched according to the patterned hard mask layer 18. This step typically involves etching of the polysilicon layer 16 using a gas mixture including chlorine, oxygen, helium and bromine. Accordingly, the polysilicon layer 16, which is etched according to the hard mask layer 18, remains on the gate oxide layer 14, as shown in Figure 1B.

[0010] As further shown in Figure 1B, a problem which frequently results in the etching of the polysilicon layer 16 using a chlorine-based etchant gas mixture is that a neck 17 forms in the upper end portion of the polysilicon layer 16. This necking or notched profile is undesirable since optimum semiconductor fabrication requires that the sidewalls 16a of the etched polysilicon layer 16 be as straight and uniform as possible. Accordingly, a novel method is needed for the fabrication of a polysilicon gate in such a manner that the incidence of a necking or notched configuration formed in the

polysilicon gate layer is eliminated or at least substantially reduced.

[0011] An object of the present invention is to provide a novel method for fabricating a polysilicon gate.

[0012] Another object of the present invention is to provide a novel method for fabricating a polysilicon gate using a hard mask.

[0013] Still another object of the present invention is to provide a novel method for fabricating a polysilicon gate having substantially uniform sidewalls.

[0014] A still further object of the present invention is to provide a novel polysilicon gate fabrication method which eliminates or at least substantially reduces the incidence of a necking or notched profile in polysilicon gate layers.

[0015] Yet another object of the present invention is to provide a novel polysilicon gate fabrication method which includes patterning a hard mask on a polysilicon layer and etching the polysilicon layer according to the patterned hard mask using a fluorine-based etchant gas.

[0016] Another object of the present invention is to provide a novel polysilicon gate fabrication method which may include patterning a hard mask on a polysilicon layer and etching the polysilicon layer in a two-step etch process.

[0017] Still another object of the present invention is to provide a novel polysilicon gate fabrication method which may include etching of a polysilicon layer using a fluorine-based etchant gas followed by etching of the polysilicon layer using a non-fluorine-based etchant gas to eliminate or at least substantially reduce the tendency to form a necking profile in the polysilicon layer.

Summary of the Invention

[0018] In accordance with these and other objects and advantages, the present invention is generally directed to a novel method for fabricating a polysilicon gate on a substrate. The method includes fabricating a multi-layered semiconductor structure including a substrate on which is sequentially fabricated a gate oxide layer, a polysilicon layer, a hard mask layer, and a resist layer which may include a bottom anti-reflective coating (BARC) layer. The hard mask layer is etched according to the patterned resist layer, after which the resist layer is stripped from the mask layer. Using a fluorine-based

etchant gas mixture, the polysilicon layer is then etched according to the mask layer. The resulting sidewall profile of the etched polysilicon layer is substantially straight, uniform and devoid of a necking or notched configuration.

[0019] In accordance with the present invention, the polysilicon layer may be etched according to a two-step etch process. In the first etching step, the polysilicon layer is partially etched using a fluorine-based etchant gas. In the second etching step, etching of the polysilicon layer is completed using a non-fluorine-based etchant gas. The non-fluorine-based etchant gas may be an etchant gas mixture which includes chlorine, oxygen, helium and bromine, for example.

Brief Description of the Drawings

[0020] The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

[0021] Figures 1A and 1B are cross-sectional views of a multi-layered semiconductor structure, illustrating a typical conventional technique for fabricating a polysilicon gate;

[0022] Figures 2A-2F are cross-sectional views of a multi-layered semiconductor structure, illustrating fabrication of a

polysilicon gate according to the method of the present invention; and

[0023] Figure 3 is a flow diagram illustrating a typical flow of sequential process steps according to the method of the present invention.

Detailed Description of the Invention

[0024] The present invention contemplates a novel method for fabricating a polysilicon gate on a substrate. According to the method, a multi-layered semiconductor structure is initially fabricated on a substrate. The multi-layered semiconductor structure typically includes a substrate, a gate oxide layer provided on the substrate, a polysilicon layer provided on the gate oxide layer, a hard mask layer provided on the polysilicon layer, and a resist layer provided on the hard mask layer. A bottom anti-reflective coating (BARC) layer may be provided between the hard mask layer and the resist layer.

[0025] After fabrication of the multi-layered semiconductor structure, the hard mask layer is etched according to the patterned resist layer. The resist layer is then stripped from the mask layer. The polysilicon layer is then etched according to the mask layer, an etchant gas mixture which includes

fluorine. The fluorine-based etching process imparts a substantially uniform sidewall profile, which is substantially devoid of a necking or notched configuration, to the etched polysilicon gate layer.

[0026] In accordance with the present invention, the polysilicon layer may be etched according to a two-step etch process, in which etching of the layer is begun in the first step and completed in the second step. The first etching step is carried out using a fluorine-based etchant gas. The second etching step is carried out using a non-fluorine-based etchant gas, which may be an etchant gas mixture that includes chlorine, oxygen, helium and bromine, for example.

[0027] Referring next to Figures 2A-2F, in conjunction with the flow diagram of Figure 3, wherein sequential process steps are carried out to fabricate a polysilicon gate according to the method of the present invention. As shown in Figure 2A and step S1 of Figure 3, a multi-layered semiconductor structure 30 is initially formed on a substrate 32. The multi-layered semiconductor structure 30 includes a gate oxide layer 34 deposited on the substrate 32, a polysilicon layer 36 deposited on the gate oxide layer 34, a hard mask layer 38 deposited on the polysilicon layer 36, a bottom anti-reflective coating (BARC)

layer 40 optionally deposited on the hard mask layer 38, and a patterned resist layer 42 deposited on the BARC layer 40.

[0028] The substrate 10 is typically a silicon semiconductor wafer and may include active and passive IC devices fabricated within the wafer. Additionally or alternatively, devices may be fabricated in layers formed on the wafer. The substrate 10 may be a semiconductor wafer of any size; for example, an eight- or twelve-inch diameter wafer. The gate oxide layer 34 is preferably silicon dioxide and has a thickness of typically about 10~100 angstroms.

[0029] The polysilicon layer 36 is typically a poly-crystalline layer of silicon that is deposited on the gate oxide layer 34. The polysilicon layer 36 can function as a silicon gate or can be used as an interconnection between IC devices. The polysilicon layer 36 preferably has a thickness of typically about 500~3000 angstroms. The polysilicon layer 36 may further include a WSi_x or other refractory metal layer (not shown).

[0030] The polysilicon layer 36 may be either pre-doped or amorphous silicon. After deposition of the polysilicon layer 36 on the gate oxide layer 34, the the polysilicon layer 36 may be annealed to cause diffusion of dopant ions throughout the

polysilicon layer 36. The polysilicon anneal step also activates the chemical bonds between the dopant atoms and the silicon atoms in the polysilicon, such that the dopant atoms become a part of the crystalline polysilicon lattice structure in a process known as electrical activation. Alternatively, the polysilicon anneal step may be omitted.

[0031] The hard mask layer 38 is preferably silicon oxide, silicon nitride or silicon oxynitride. Most preferably, the hard mask layer 38 is silicon oxide. The hard mask layer 38 preferably has a thickness of typically about 200~3000 angstroms. The BARC layer 40 is preferably a polymer resin with photo compounds and has a thickness of typically about 200~2000 angstroms.

[0032] The resist layer 22 is formed over the BARC layer 40 and patterned, exposed and developed to form the pattern that defines the polysilicon gate and other device structures to be fabricated on the substrate 12. The resist layer 22 is preferably a DUV positive photoresist such as IBM APEX resist, IBM KRS resist, Hoechst Ax's DX-46, OCG's ARCH resists, Shinetsu, Tok, AZ or JSR. The resist layer 22 can be any photoresist material such as a negative photoresist, and preferably has a

thickness of typically about 1000~10000 angstroms and a width of typically about 0.05~0.30 μm.

[0033] As shown in Figure 2B and process step S2 of Figure 3, the BARC layer 40 is next etched according to the patterned resist layer 42. The etching process for the BARC layer 40 is carried out typically in a high density plasma (HDP) etcher, using a transformer coupled plasma (TCP) etch reaction with bromine and oxygen. Typical process parameters for the reaction are as follows: chamber pressure (5~30 mTorr, preferably, 10 mTorr); TCP power (100~1500 W, preferably, 250 W); bias power (100~1500 W, preferably, 250 W); HBr flow rate (50~300 sccm, preferably, 50 sccm); O_2 flow rate (5~100 sccm, preferably, 15).

[0034] As shown in Figure 2C and process step S3 of Figure 3, the hard mask layer 38 is then etched according to the patterned resist layer 42. The etching process for the hard mask layer 38 is carried out typically in an HDP etcher using a TCP etch reaction with fluorocarbon (C2F6, CF4). Typical process parameters for the reaction are as follows: chamber pressure (5~30 mTorr, preferably, 10 mTorr); TCP power (100~1500 W, preferably, 300 W); bias power (100~1500 W, preferably, 250 W); C_2F_6 flow rate (30~300 sccm, preferably, 100 W).

[0035] As shown in Figure 2D and process step S4 of Figure 3, the resist layer 42 and the underlying BARC layer 40 are stripped from the polysilicon layer 36. Accordingly, the patterned and etched hard mask layer 38 remains on the upper surface of the polysilicon layer 36. The resist and BARC stripping process is carried out in an HDP chamber, typically a TCP reactor with separate source and bias control. A biased O_2 plasma is used to strip the BARC layer 40 from the hard mask layer 38. A small quantity of C_2F_6 may be added to the process to enhance stripping of the BARC layer 40, as deemed necessary. Typical process parameters for the stripping process are as follows: chamber pressure (5~80 mTorr, preferably, 20 mtorr); TCP power (100~1500W mTorr, preferably, 300W mtorr); bias power (100~1500W Ttorr, preferably, 0 mTorr); O_2 flow rate (50~500 sccm, preferably, 200 sccm).

[0036] After etching of the BARC layer 40, as shown in Figure 2B and step S2; etching of the hard mask layer 38, as shown in Figure 2C and step S3; and stripping of the resist layer 42 and BARC layer 40, as shown in Figure 2D and step S4, the polysilicon layer 36 is etched according to the pattern defined by the hard mask layer 38. According to the method of the present invention, a fluorine-based etchant gas is used to etch the polysilicon layer 36. Preferably, the polysilicon layer 36 is etched using a

two-step etch process, which includes a partial-etch step in which a fluorine-based etchant gas is initially used to partially etch the polysilicon layer 36. This is followed by a complete-etch step in which a non-fluorine-based etchant gas is used to complete etching of the polysilicon layer 36.

[0037] Referring next to Figure 2E and step S5 of Figure 3, in the partial-etch step, a fluorine-based gas is used to partially etch the polysilicon layer 36 according to the pattern defined by the patterned and etched hard mask layer 38. The fluorine-based etching process is typically carried out in a high density plasma (HDP) etch chamber. The fluorine-based etchant gas may include a gas such as fluorocarbon, fluoronitride or fluorosulfur, in non-exclusive particular. Application of the fluorine-based etchant gas in the partial etch step is typically followed by the complete etch step, which utilizes an etchant gas devoid of fluorine and typically having chlorine, bromine, oxygen and helium to enhance etching profile uniformity in the sidewalls of the etched polysilicon layer 36.

[0038] Typical process parameters for the fluorine-based partial-etch step S5 include a chamber pressure of typically from about 5 mTorr to typically about 80 mTorr; a source radio frequency of from typically about 100 watts to about 1500 watts

at a source radio frequency of 13.56 MHz; a bias power of from typically about 50 to typically about 1500 watts; and a fluorine-based etchant gas flow rate of typically about 100 sccm.

[0039] After the fluorine-based partial-etch step S5 is completed, the partially-etched polysilicon layer 36 of Figure 2E is typically subjected to the non-fluorine-based complete-etch step S6, as shown in Figure 2F. In the complete-etch step, a non-fluorine-based etchant gas, or etchant gas devoid of fluorine, is used to complete the etching of the polysilicon layer 36 which was begun in the fluorine-based partial-etch step of Figure 2E and step S5. In the complete-etch step, etching of the polysilicon layer 36 is completed according to the pattern defined by the mask layer 38.

[0040] Like the partial-etch step S5, the complete-etch step S6 is typically carried out in a high density plasma (HDP) etch chamber. The non-fluorine-based etchant gas may include a gas mixture of chlorine, oxygen, helium and bromine, for example. After completion of the complete-etch step of the etching process, the sidewalls 36a of the etched polysilicon layer 36 are substantially uniform, vertical and devoid of a necking or notched profile which characterizes conventional hard mask polysilicon etching processes, as shown in Figure 2F.

[0041] Typical process parameters for the non-fluorine-based complete-etch step S6 include a chamber pressure of typically about 5~30 mTorr, and preferably, about 10 mTorr; a source radio frequency of typically about 100~1500 watts, and preferably, about 150 watts, at a source radio frequency of 13.56 MHz; a bias power of typically about 100~1500 watts, and preferably, about 150 watts; a Cl_2 gas flow rate of typically about 20~500 sccm, and preferably, about 50 sccm; a He gas flow rate and an O_2 gas flow rate of typically about 10~500 sccm, and preferably, about 15 sccm; and an HBr gas flow rate of typically about 10~500 sccm, and preferably, about 150 sccm.

[0042] While the preferred embodiments of the invention have been described above, it will be recognized and understood that various modifications can be made in the invention and the appended claims are intended to cover all such modifications which may fall within the spirit and scope of the invention.